



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,920	10/21/2003	Woo Hyun Kim	041501-5458-01	3193
26633	7590	08/10/2005	EXAMINER	
HELLER EHRMAN WHITE & MCAULIFFE LLP 1717 RHODE ISLAND AVE, NW WASHINGTON, DC 20036-3001			DUONG, THOI V	
			ART UNIT	PAPER NUMBER
			2871	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/688,920

Applicant(s)

KIM ET AL.

Examiner

Thoi V. Duong

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 25 is/~~are~~ pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/~~are~~ withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/~~are~~ allowed.
- 6) ☒ Claim(s) 25 is/~~are~~ rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/~~are~~ objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/~~are~~: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 10/012.395
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 02, 2005 has been entered.

Accordingly, claim 25 was amended and claims 1-24 were cancelled. Currently, claim 25 is pending in this application.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 25 is rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al (USPN 5,969,779).

As shown in Figs. 7, 8 and 10, Kim et al. discloses a liquid crystal display (LCD) panel comprising:

an insulating substrate 21 (see also Fig. 4) defined as a cell region 3 (display region) and a pad region (outside display region);

a plurality of gate lines G1-Gm formed in the cell region;

a plurality of data lines D1-D2n crossing the gate lines and having alternately different extended lengths to the pad region (Fig. 7 with a diagram illustrating portion 7 and Fig. 8),

wherein alternately different extended lengths are also respectively at alternately and completely different levels above the insulating substrate as seen from Fig. 10, where the extended data line D2n-1 is formed on a semiconductor layer 25' over a gate insulating layer 24 and the extended data line D2n is formed on the gate insulating layer 24 only; and

data pads (input pads) 1, 1' applying an electric signal to the data lines (col. 1, lines 10-23 and 45-53).

#### ***Response to Arguments***

4. Applicant's arguments filed June 02, 2005 have been fully considered but they are not persuasive.

Applicant argued that Kim does not teach or suggest "a plurality of data lines crossing the gate lines having alternately different extended lengths to the pad region, wherein alternately different extended lengths are also respectively at alternately and completely different levels above the insulating substrate." The Examiner disagrees with Applicant's remarks since, in the pad region of data lines D1-D2n (outside the display region 3), the data lines, for example D2n-1 and D2n, cross the gate lines G1-Gm and have alternately different lengths extended from the display region 3 to the pad region as clearly shown in a diagram illustrating portion 7 in Fig. 7 and Fig. 8. And, as shown in Fig. 10 which is a sectional view of Fig. 8 along a 9-9 section line, the extended data

Art Unit: 2871

line D2n-1 is disposed on a level comprising a semiconductor layer 25' and a gate insulating layer 24 and the extended data line D2n is formed only on the gate insulating layer 24. Accordingly, the alternately different extended lengths of the data lines D2n-1 and D2n are also respectively at alternately and completely different levels above the insulating substrate. Thus, Kim does teach the claimed invention.

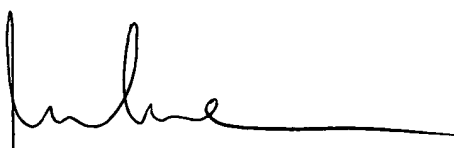
**Conclusion**

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong

08/06/2005



DUNG T. NGUYEN  
PRIMARY EXAMINER